CHIP SCALE THERMAL MANAGEMENT OF HIGH BRIGHTNESS LED PACKAGES

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ABSTRACT

The efficiency and reliability of the solid-state lighting devices strongly depend on successful thermal management. Light emitting diodes, LEDs, are a strong candidate for the next generation, general illumination applications. LEDs are making great strides in terms of lumen performance and reliability, however the barrier to widespread use in general illumination still remains the cost or $/Lumen. LED packaging designers are pushing the LED performance to its limits. This is resulting in increased drive currents, and thus the need for lower thermal resistance packaging designs. As the power density continues to rise, the integrity of the package electrical and thermal interconnect becomes extremely important. Experimental results with high brightness LED packages show that chip attachment defects can cause significant thermal gradients across the LED chips leading to premature failures. A numerical study was also carried out with parametric models to understand the chip active layer temperature profile variation due to the bump defects. Finite element techniques were utilized to evaluate the effects of localized hot spots at the chip active layer. The importance of "zero defects" in one of the more popular interconnect schemes; the "*epi down*" soldered flip chip configuration is investigated and demonstrated.

Keywords: High brightness LEDs, Infrared imaging, Microscopic IR, Bump defects, Finite element analysis.

INTRODUCTION

According to the Haitz's law, a high brightness LED package flux doubles in every 18-24 months. This trend has continued for the last 30 years (Lumileds, 2004). The contributors to this increase include improvements in epitaxial growth, LED design, and higher drive currents. Solid-state lighting package heat generation rates are comparable to IC's (i.e. Integrated circuits) trends and needs. In fact today, LEDs surprisingly require more aggressive cooling techniques. Based on the International Technology Roadmap for Semiconductors [ITRS Report, 2003], total power consumption continues to increase due to the higher chip operating frequencies, and higher interconnect capacitance and resistance, as well as the increasing gate leakage. The chip heat fluxes are expected to be in excess of 70 W/cm^2 by the end of this decade, and about 100 W/cm^2 by 2018. Heat flux from a 900 μm square high brightness LED chip, has already reached

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approximately 125 W/cm^2. For the last several years, various papers have been published about solid-state lighting thermal problems. Thermal problems in high brightness LED packages and systems was studied by Arik et al [2001]. The authors provided a general discussion paper about package and system level problems. Later, another paper about thermal considerations in the LED phosphor particles and layers was published by Arik et al [2003]. The current study focuses on the chip scale thermal management of LEDs to identify some of the key thermal challenges and problems.

To be practical for general illumination, LED systems must reach 1200-1500 lumen levels at acceptable costs while maintaining reliability. It is estimated that 80 percent of the cost of an LED illumination system is attributed to the die cost. Improvements in the epitaxial growth and LED design will ultimately be the long-term solution. In the near term higher drive currents and innovative packaging solutions will provide the maximum extraction from the LEDs. This trend is evident in commercially available devices where power densities have recently tripled while still maintaining the LED efficiency and reliability. To accomplish these goals, smart packaging solutions, that keep the die junction temperature at a minimum and light extraction at a maximum, are necessary. This has led to a general trend of "epi down" flip chip packaging to minimize the thermal path length and improve light extraction.

The typical LED packaging configuration is flip chip soldering of the LED device to a silicon submount. The silicon submount provides the electrical interconnect to the die as well as electrostatic zener protection. The submount is then secured within the package and wire bonded to the package leadframe In order to maximize the heat extraction; the contact area from the submount to the die must be maximized. This requires an increase of the size and/or number of electrical interconnects in the LED packages. This requirement must be balanced with the fact that increasing the number of contacts increases die stress and has the potential to reduce packaging yields and reliability. Poor contacts to the die do not always manifest themselves in initial electrical or lumen testing. However, these poor contacts can result in localized heating on the LED and have a major impact on long-term reliability. The reliability of the LED, due to the local heating suffers both in the epitaxial layer and the epoxy encapsulation. The end result is accelerated loss of lumen output or ultimately premature device failure.

In this paper actual as well as molded results showing the importance of the interconnect integrity will be discussed. An experimental study to obtain chip temperatures from various chip designs was completed. A numerical analysis through Finite element models was carried out. Results from experimental and numerical studies will be presented in graphical form.

CHIP SCALE THERMAL MANAGEMENT

Experimental Study: Thermal Gradients at Various LED Chips

Various types of LED chip designs such as vertical or horizontal, continuous or finger/bumps, sapphire or SiC substrates are available. While simple at first glance, a typical LED device is made up of many complex proprietary layers. While building a defect free chip is a major challenge, placing it in a reliable package brings on mechanical and

operational challenges. While mechanical problems arise from CTE and elasticity module mismatches, operational problems arise from thermal cycles, harsh environments and over-driving conditions.

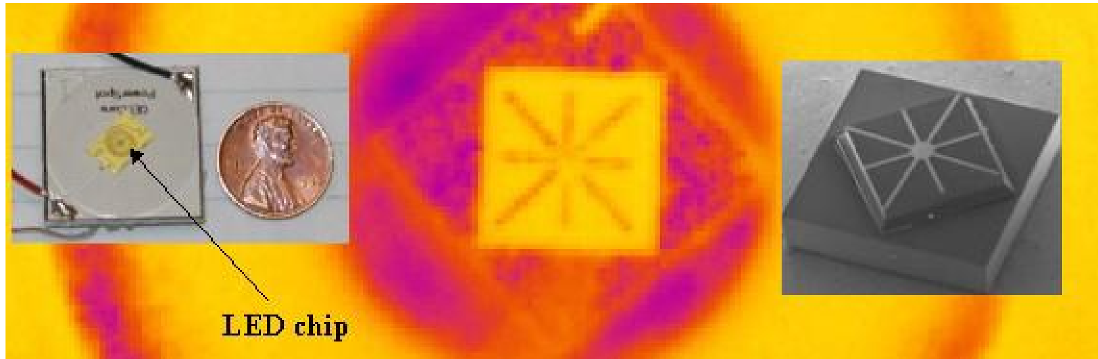

Figure 1. Infrared and digital images of a high brightness LED package.

Figure 1 shows various images of a high brightness LED device housed in a package. On the left, the chip is housed in a package and it's size compared with a penny. With a naked eye it is almost impossible to notice the existence of the chip. The center and background images were taken from a microscopic Infrared thermal image of the package and chip. The image on the right side is a close up digital image of the chip. It is interesting that the IR camera was able to capture the finger structures on the LED surface. The primary interest of this study was to identify the chip temperature distribution. Thermal gradients will be discussed in the following paragraphs for various chips and orientations.

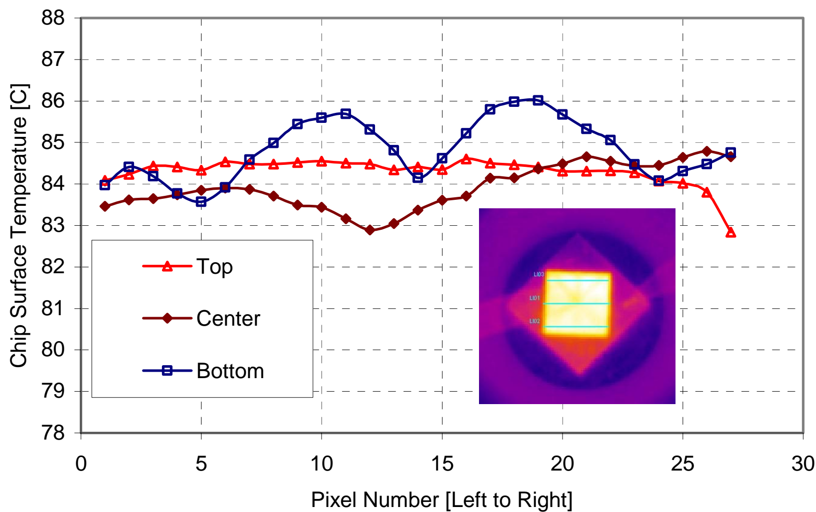

Figure 2. IR thermal image of a good contact LED chip

A good thermo-mechanical bonding of the chip results in uniform temperatures as given in Figure 2. The surface of the LED package as well as the chip was coated with a known emissivity phosphor layer. The microscopic infrared

thermal imaging and the calibration of coating material are described in Garg et al [2004]. The maximum temperature observed was about 86 °C, while the temperature gradient was approximately 3 °C.

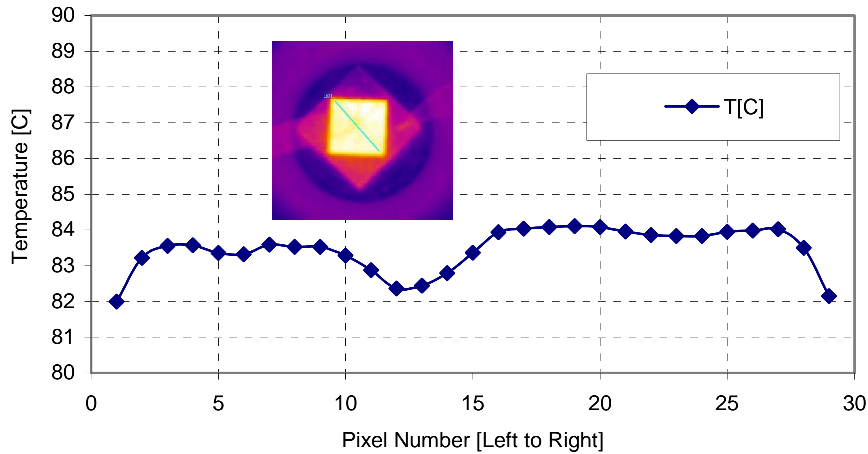

Figure 3. Temperature distribution in a good package

The microscopic IR camera enables thermal scientists to measure as small as 30 µm pixel sizes. In other words, for a 905 µm square chip, an array of 30x30 pixels is available. The chip was tilted at a slight angle to avoid reflections back into the camera. The image in Figure 2 shows a very uniform temperature profile due to several reasons. First, the chip anode has nearly total coverage of the active or epi layer, the substrate is highly thermally conductive (SiC) and the chip to submount attach is uniform and void free. Additionally the architecture and manufacturing of the package plays a significant role in achieving uniform chip temperatures. For this discussion we will concentrate on the die and surmount utilizing high resolution IR imaging.

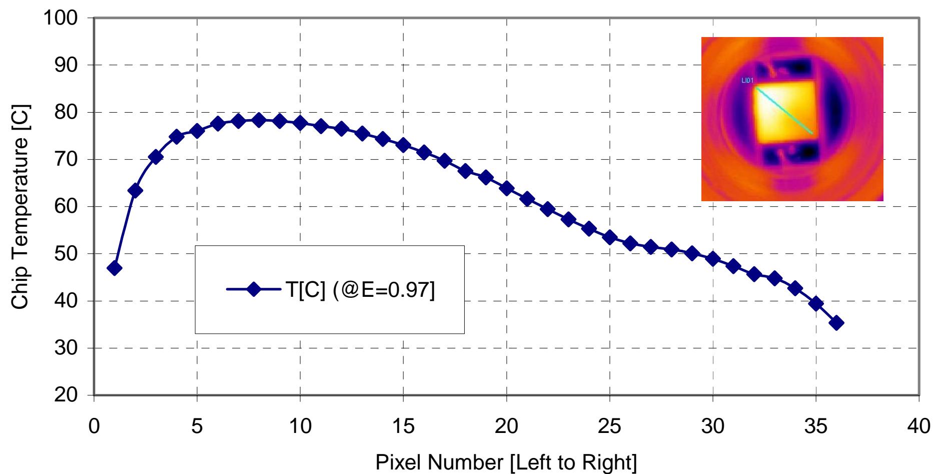

Figure 4. Temperature distribution of a high brightness defective LED chip in a power package.

Temperature distribution shown across the diagonal for another good package is given in Figure 3. While one pixel from left and right sides shows the effect of convective heat transfer from sides, the rest of the chip seems to be within $\pm$ 1 °C. This is an expected result from the thermal models as well. It should be noted from Figure 1 through 3 that if the chip has a good active layer design, and the package design is thermally efficient and defect free, the temperature profile across the chip should not exceed a couple of degrees. In the following sections, this technique will be used to identify defects in individual LED devices in a package.

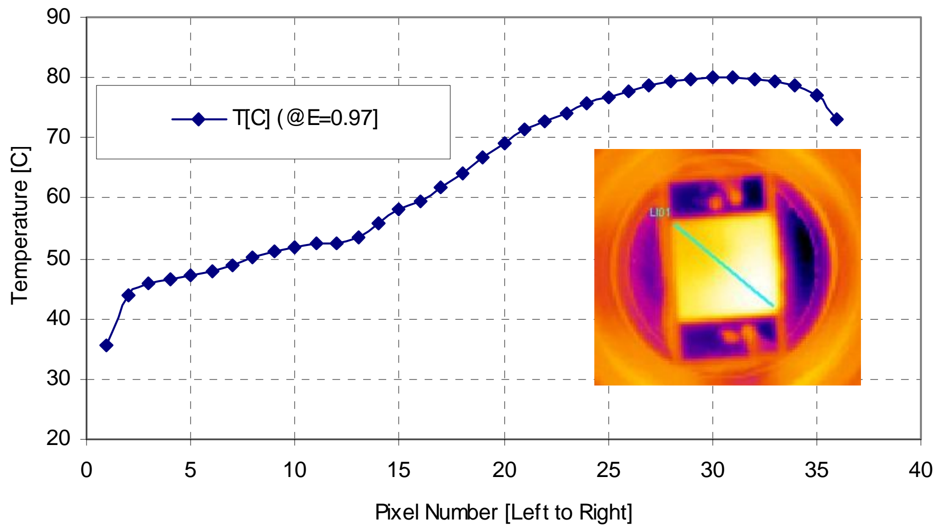

Figure 5. Temperature distribution for the defective LED package (rotated 180° from Figure 4)

A problematic, sapphire based, high brightness LED power package temperature distribution is given in Figure 4. This device was identified as having excessive lumen loss during “HTOL” (High Temperature Operating Life) testing. Due to subsequent testing needs no emissivity coating was implemented for this package. An estimated emissivity of 0.97 was used for the sapphire substrate at a camera wavelength of 8 μm (long wavelength). The primary goal of this study was obtaining relative temperature differences to understand defects in either the chip, package, or perhaps both. From the figure it can be seen that a 43 °C temperature gradient exists across this LED chip. This indicates serious problems at either the chip or the package level.

One can argue that the thermal gradient might be due to the natural convection effect and the orientation of the chip during measurement. In other words, hot air rises and upper parts of the chip may experience warmer air than the bottom. In fact the chip size is less than $1mm^2$, so this should not be a concern. However, to determine if there were any effects due to the orientation a further test was performed by rotating the chip 180° around the normal axis. These measurements show negligible difference from the previous suggesting that the gradient is indeed real. Several factors were investigated to determine the cause of the gradient and failure. Prior to obtaining these IR images an electrical and physical examination of the device was completed and no anomalies were discovered. The LED encapsulant was then removed by solvent soaking and checked at various stages during the de-encapsulation. Epoxy darkening close to the

chip surface was observed. This darkening aligns with the observed high temperature portion of the IR thermal images, suggesting premature failure of the epoxy due the high temperatures. A further study to check the chip to submount bonding was performed. Figure 6 shows a microscopic image of the chip to submount bonding surface. It is clear that some of the bumps did not have good contact between the chip and the submount. This non-contact would account for poor local thermal performance and thus localized hot spots on the chip.

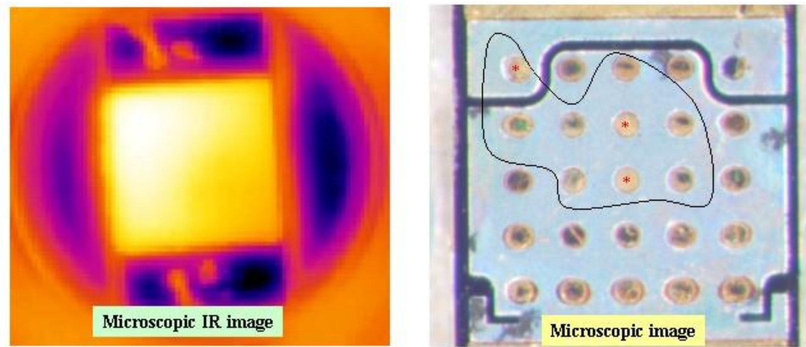

Figure 6. Further package analysis: IR image vs. microscopic image

Chip Thermal Models: Predicting Hot Spots

To further understand the thermal impact of the chip to submount interconnects, Finite Element thermal models were constructed using ANSYS8.0 [Ansys8.0 Manual, 2004]. Figure 7 represents the idealized FEM model of the chip and package. A square HB LED chip with a size length of approximately 900 μm was created. Interconnect bumps are used for both electrical and thermal reasons. The bumps are evenly distributed under the chip and 25 bumps are established. The radius of each bump is 40 μm while the bump heights are chosen to be 25 μm. The submount to conductive circular structure is connected via a solder layer. To simplify the model heat flux is applied uniformly at the bottom of the chip surface where the active layer is located. Keep in mind that chip layouts will determine current spreading and thus determine the actual distribution of the heat. A convective boundary condition at the backside of the conductive substrate is implemented to obtain the temperature gradient in the chip and other parts of the system.

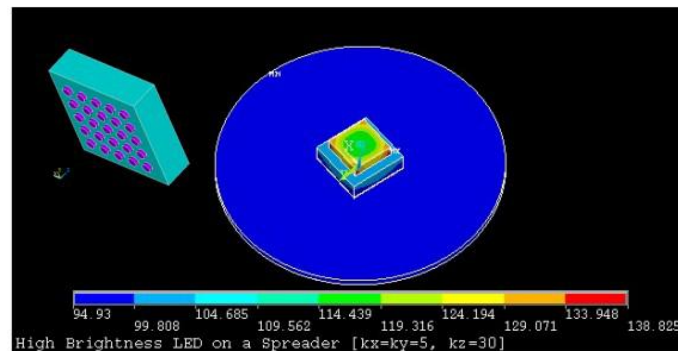

Figure 7. ANSYS FEM model for the HB LED chip.

There are a couple of popular choices for the LED chip substrate. The substrate can be very conductive, such as SiC (k=400 W/m^2-K), or a ceramic based material such as Sapphire (k=30 W/m^2-K) with a comparably lower thermal conductivity. A parametric study to understand the effect of the substrate thermal conductivity was carried out. In Figure 8, the chip thermal conductivity in the xy plane was varied between 5 and 400 W/m^2-K. The chip orthogonal (z-axis) thermal conductivity was was held constant at 30W/m^{2}K. A typical sapphire based device is represented by the isotropic values (k_x=k_y=k_z=30 W/m^2-K) enclosed in the oval. Even for a defect free attachment a variation of 10 °C can be expected across the chip in the non bump areas.

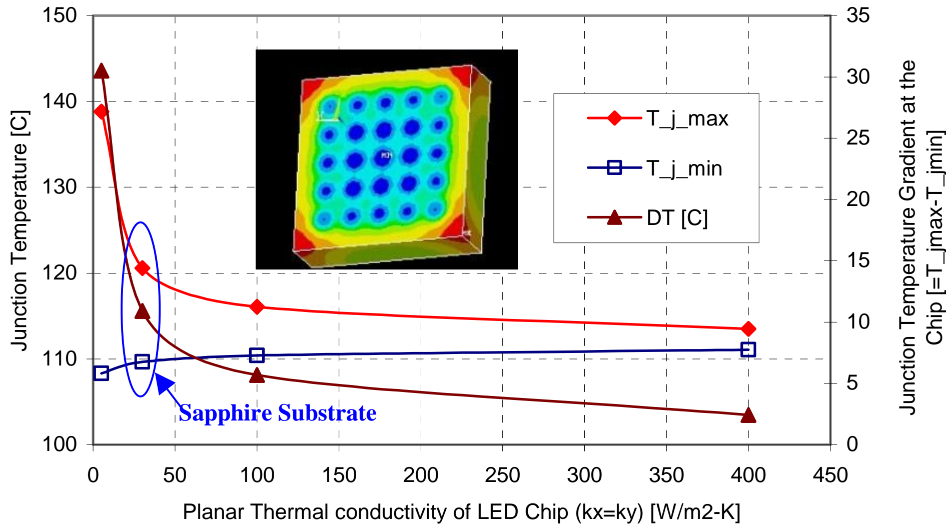

Figure 8. Effect of planar thermal conductivity of the LED chip for k_z=30 W/m^2-K.

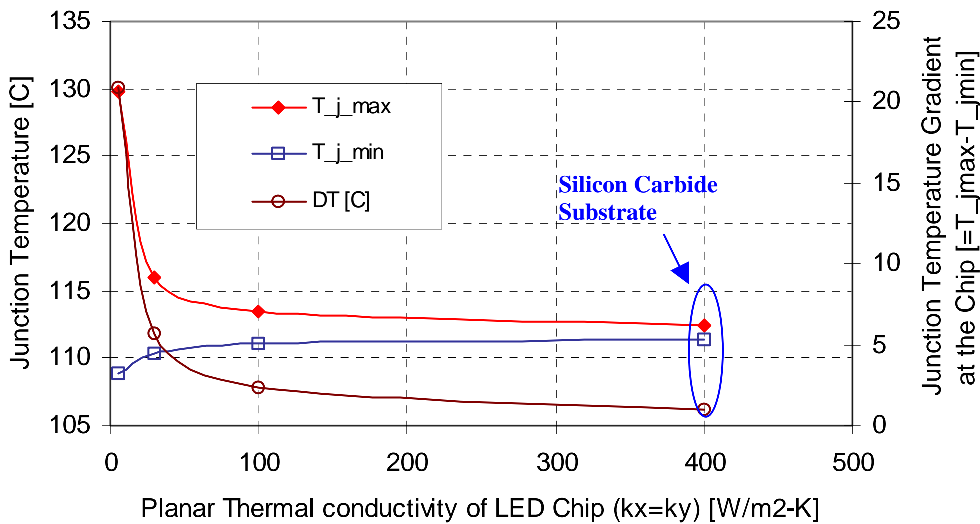

Figure 9. Effect of planar thermal conductivity of the LED chip for kz=400 W/m^2-K.

In Figure 9, the chip thermal conductivity in the xy plane was again varied between 5 and 400 W/m^2-K. The chip orthogonal (z-axis) thermal conductivity was held constant at 400 W/m^2-K. A typical silicon carbide device is represented by the isotropic values ($k_x=k_y=k_z=400$ W/m^2-K) enclosed in the oval. Due to the higher thermal conductivity, thus greater lateral thermal spreading, a reduction in the thermal gradient across the chip to 1 °C is observed in the non-bump areas.

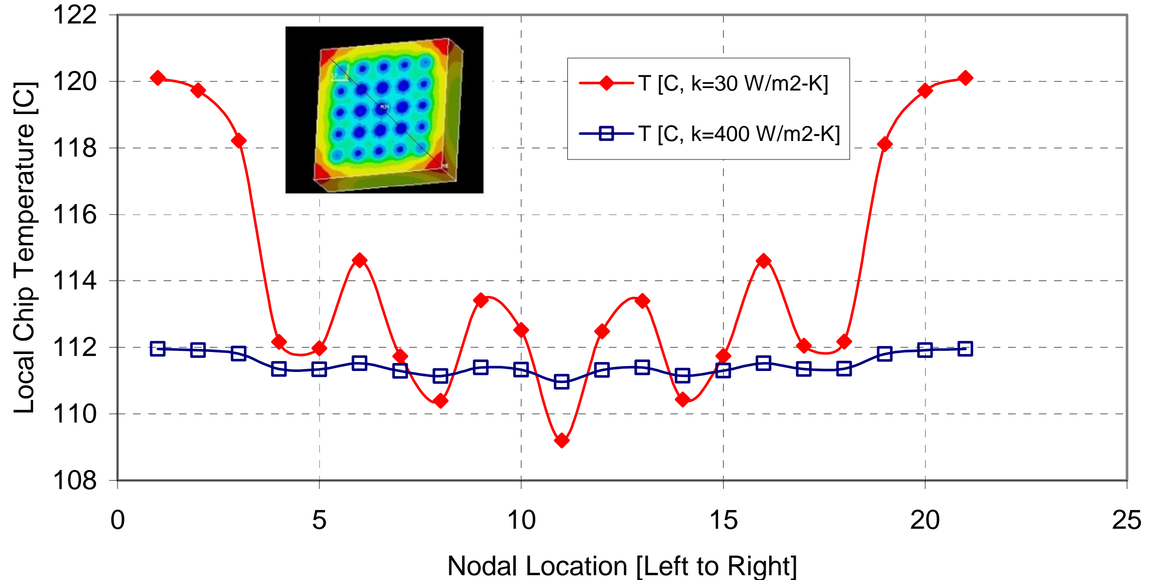

Figure 10. Temperature distribution across the diagonal of the chips

In order to provide a more detailed analysis, both the non-bumped and bumped areas of the chip need to be investigated. The bumps provide the electrical as well as the thermal connection for the LED device. The temperature gradient across the diagonal, through the bumps, of a silicon carbide and sapphire based chip is given in Figure 10. It is interesting to see the significant difference in temperature gradients across the chips. As expected the silicon carbide based device has much less variation. Also in general the bump locations have lower temperatures, while the corners experienced much higher temperatures. This again iterates the importance of the substrate material, the bump placement, and density on the active area.

Figure 11 represents the typical bump layout for a good and defect containing HB LED chip The left side of the figure has 25 perfect bumps, while right side has 21 good and 4 defective bumps ($k=10^{-6}$ W/m^2-K). Four bad connections correspond to only 16% of the total bump area yet the effect can be quite serious in thermal behavior.

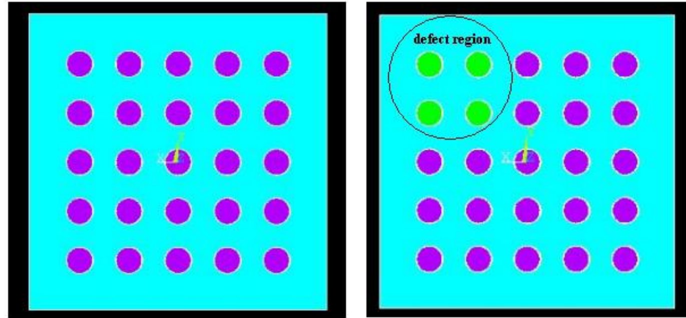

Figure 11. Defect free and defective bumps for a typical LED chip.

Figure 12 represents the temperature distribution for silicon carbide and sapphire based chips with 4 defective bumps. As expected the left top corner of the chip experiences much higher temperatures than other sections of the chip. The maximum temperature gradient of 22 °C occurs in the sapphire based chip and is approximately 11X greater than the silicon carbide based device. The result for the sapphire based chip is a best-case approximation because the model assumes perfect, current or heat, spreading in the active layer. In real devices the current or heat spreading is directly dependent upon the LED design and varies amongst manufacturers. The temperature variation and the maximum temperature in a real device could be much higher and are more than likely to lead to reliability issues. The silicon carbide device shows little impact due to the defective bumps because of its high lateral thermal spreading. A further study would be necessary to determine what defect levels would effect the silicon carbide devices.

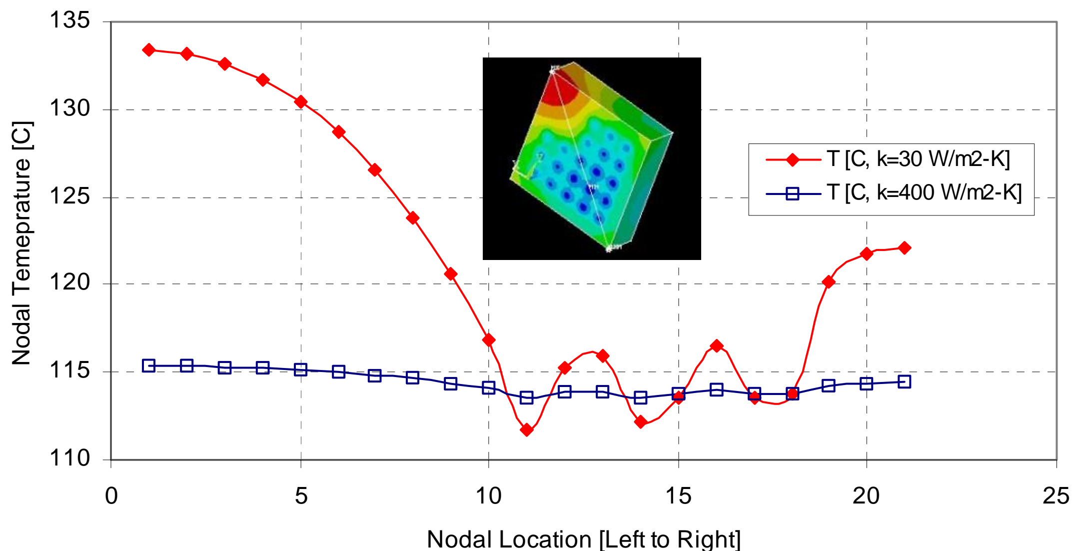

Figure 12. Temperature distribution along the diagonal for isotropic substrates.

A numerical and experimental study to understand the thermal behavior of typical high brightness LED chips as it relates to die attach was completed. It is observed that the thermal conductivity of the substrate material and the bump layout play a significant role in the chip thermal distribution, which relates directly to device lifetimes and failure modes. It should be appreciated that there are many ways of designing chips and creating bump layouts. An extensive DOE (i.e. design of experiments) would be required to understand the thermal behavior of the chip including bump material, radius, height, locations, and density, as well as the submount material.

SUMMARY AND CONCLUSIONS

A study to understand the chip level temperature distribution was completed. In this study, details within the chip active layer were not investigated, however lumped models were established to provide guidance to both chip designers and packaging engineers. A well-designed LED chip and package would experience the lowest temperature gradients, while a poor chip design with packaging defects can lead to serious problems for both the optical efficiency, and reliability. Microscopic IR measurements were completed using a state of the art system, which enables very fine pixel sizes as small as 30 μm. Thermal models through finite element technique were established for a fictitious typical LED chip and package design. Effects of the substrate thermal conductivities and bump defects were studied with parametric models and actual packages.

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